IN THE CLAIMS

1 (Currently Amended). A method comprising:

defining a multilevel cache including a core having relatively faster components and a region including relatively slower components; and

implementing a line replacement policy ~~performing virtual-to-physical translation~~ in said region.

2 (Original). The method of claim 1 including managing the core from a level 2 cache.

3 (Original). The method of claim 1 including using a virtual address to index the core to avoid the need for an address translation mechanism.

4 (Original). The method of claim 1 including placing functions relating to tags and valid bits as well as the data itself in the core.

5 (Original). The method of claim 1 including using a write-through core cache.

6 (Currently Amended). The method of claim 1 including performing virtual-to-physical translation ~~implementing a line replacement policy~~ in said region.

Claim 7 (Canceled).

8 (Previously Presented). The method of claim 1 including handling a core cache miss by passing details of an access to said region.

9 (Original). The method of claim 8 including enabling said region to use a memory translation mechanism to determine the physical address and attributes of the access.

10 (Previously Presented). The method of claim 9 including checking to see if requested data is in a storage associated with said region.

11 (Currently Amended). An article comprising a medium storing instructions that, if executed, enable a processor-based system to:

define a multilevel cache including a core having relatively faster components and a region including relatively slower components; and

implement a line replacement policy ~~perform virtual-to-physical translation~~ in said region.

12 (Original). The article of claim 11 further storing instructions that enable the processor-based system to manage the core from a level 2 cache.

13 (Original). The article of claim 11 further storing instructions that enable the processor-based system to use a virtual address to index the core to avoid the need for an address translation mechanism.

14 (Original). The article of claim 11 further storing instructions that enable the processor-based system to access functions relating to tags and valid bits as well as the data itself in the core.

15 (Original). The article of claim 11 further storing instructions that enable the processor-based system to use a write-through core cache.

16 (Currently Amended). The article of claim 11 further storing instructions that enable the processor-based system to perform virtual-to-physical translation ~~implement a line replacement policy~~ in said region.

Claim 17 (Canceled).

18 (Previously Presented). The article of claim 11 further storing instructions that enable the processor-based system to handle a core cache miss by passing details of an access to said region.

19 (Original). The article of claim 18 further storing instructions that enable the processor-based system to enable said region to use a memory translation mechanism to determine the physical address and attributes of the access.

20 (Previously Presented). The article of claim 19 further storing instructions that enable the processor-based system to check to see if requested data is in a storage associated with said region.

21 (Currently Amended). A system comprising:

a processor;

a multilevel cache including a core having relatively faster components and a region including relatively slower components; and

said region to implement a line replacement policy ~~perform virtual-to-physical translation~~.

22 (Presently Presented). The system of claim 21 wherein said core is a level 1 cache and said region is a level 2 cache.

23 (Original). The system of claim 21 wherein said storage stores instructions that enable the processor to use a virtual address to index the core to avoid the need for an address translation mechanism.

24 (Original). The system of claim 21 wherein said storage stores instructions that enable the processor to place functions relating to tags and valid bits as well as the data itself in the core.

25 (Original). The system of claim 21 wherein said core cache is a write-through cache.

26 (Currently Amended). The system of claim 21 wherein said storage stores instructions that enable the processor to perform virtual-to-physical translation ~~implement a line replacement policy in said region~~.

Claim 27 (Canceled).

28 (Previously Presented). The system of claim 21 wherein said storage stores instructions that enable the processor to handle a core cache miss by passing details of an access to said region.

29 (Original). The system of claim 28 wherein said storage stores instructions that enable the processor to enable said region to use a memory translation mechanism to determine the physical address and attributes of the access.

30 (Previously Presented). The system of claim 29 wherein said storage stores instructions that enable the processor to check to see if requested data is in a storage associated with said region.